TS-00-415
REMARKS

Examiner J. Trimmings is thanked for the thorough examination and search of the subject Patent Application. Claims 1 and 13 have been amended. Claims 7 and 19 have been canceled. The Specification has been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the Drawings for failing to comply with 37 CFR 1.84(p)(5) because they include reference signs not mentioned in the description is requested based on the Amended Specification and on the following remarks.

In Re Fig. 4 and reference 96, the Specification has been amended in the paragraph starting on page 15 and ending on page 16 to insert the reference 96 in reference to the insertion of faults.

In Re Fig. 6 and reference 132, the Specification has been amended in the paragraph starting on page 17 and ending on page 18 to change the reference "120" to "132".

The above amendments to the Specification should allow the Drawings to comply with 37 CFR 1.84(p)(5).

Reconsideration of the Drawings for failing to comply with 37 CFR 1.84(p)(5) because they include reference signs not mentioned in the description is requested based on the Amended Specification and on the above remarks.

Reconsideration of the Specification for informalities is requested based on the Amended Specification and on the following remarks.

Page 3 has been amended to correct the reference to the BIST circuit from "14" to "10". Page 18 has been amended to correct the reference to the "...further machine encoded" from "120" to "132".

Reconsideration of the Specification for informalities is requested based on the Amended Specification and on the above remarks.

Reconsideration of Claims 1-4 rejected under 35 U.S.C. 102(b) as being fully anticipated by Bo Lu (U.S. 6,012,157) is

requested based on Amended Claim 1, Canceled Claim 7, and on the following remarks.

Applicant agrees that Lu teaches a method and an apparatus for testing a RAM BIST controller. However, Lu does not teach descrambling the set of faults in the embedded memory behavioral model as is taught in the Applicant's claimed invention. To make clear this distinction, Applicant has amended Claim 1 to include the limitation formerly in Claim 7 such that Amended Claim 1 now reads:

1. (Currently Amended) A method to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device comprising:

introducing a set of faults into an embedded memory behavior model wherein said embedded memory behavior model comprises a high-level language model and wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;

thereafter simulating said built-in self-test circuit and said embedded memory behavior model wherein said built-in self-test circuit generates input data and address patterns for said embedded memory behavior model, wherein

said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said input address and data and said memory address and data are compared in said built-in self-test circuit and a fault output is generated if not matching;

de-scrambling said set of faults; and

comparing said fault output and said set of faults to verify the performance of said built-in self-test circuit.

Claim 7 has been canceled due to redundancy.

Applicant believes that Lu does not teach the element of de-scrambling the set of faults as is taught by Amended Claim 1. Therefore, Applicant further believes that Amended Claim 1 should not be rejected under 35 U.S.C. 102(b) due to Lu. Finally, Claims 2-4 represent patentably distinct, further limitations on Lu and should, therefore, be in condition for allowance if the rejection of Claim 1 is removed.

Reconsideration of Claims 1-4 rejected under 35 U.S.C. 102(b) as being fully anticipated by Bo Lu (U.S. 6,012,157) is requested based on Amended Claim 1, Canceled Claim 7, and on the above remarks.

Reconsideration of Claims 13-17 rejected under 35 U.S.C. 102(b) as being fully anticipated by Bo Lu (U.S. 6,012,157) is requested based on Amended Claim 13, Canceled Claim 19, and on the following remarks.

As stated above, Applicant agrees that Lu teaches a method and an apparatus for testing a RAM BIST controller. However, Lu does not teach a means of descrambling the set of faults in the embedded memory behavioral model as is taught in the Applicant's claimed invention. To make clear this distinction, Applicant has amended Claim 13 to include the limitation formerly in Claim 19 such that Amended Claim 13 now reads:

13. (Currently Amended) An apparatus to verify the performance of a built-in self test circuit for testing embedded memory in an integrated circuit device comprising:

an embedded memory behavior model wherein said embedded memory behavior model comprises a high-level language model;

a built-in self-test circuit model connected to said embedded memory behavior model wherein said built-in self-test circuit model generates input data and address

patterns for said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are compared to said input address and data in said built-in self-test circuit and a fault output is generated if not matching;

a means of introducing a set of faults into said embedded memory behavior model wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;

a means of simulating said embedded memory behavior model and said built-in self-test circuit model;

a means of de-scrambling said set of faults; and

a means of comparing the fault diagnosis output of said built-in self-test circuit model and said set of faults to verify the performance of said built-in self-test circuit.

Claim 19 has been canceled due to redundancy.

Applicant believes that Lu does not teach the element of de-scrambling the set of faults as is taught by Amended Claim 13. Therefore, Applicant further believes that Amended Claim 13

should not be rejected under 35 U.S.C. 102(b) due to Lu. Finally, Claims 14-17 represent patentably distinct, further limitations on Lu and should, therefore, be in condition for allowance if the rejection of Claim 13 is removed.

Reconsideration of Claims ~~1-4~~ 14-17 rejected under 35 U.S.C. 102(b) as being fully anticipated by Bo Lu (U.S. 6,012,157) is requested based on Amended Claim 13, Canceled Claim 19, and on the above remarks.

Reconsideration of Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of SyTest Technologies, Inc., March 1999, is requested based on Amended Claim 1 and on the following remarks.

Applicant believes that neither Lu nor SyTest teach or suggest, separately or in combination, the key element of de-scrambling the set of faults as is taught in Applicant's claimed invention per Amended Claim 1. Therefore, Applicant does not believe that it would have been obvious to one skilled in the art at the time of the invention to have used the teachings of Lu and/or SyTest to practice the claimed invention.

Reconsideration of Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of SyTest Technologies, Inc., March 1999, is requested based on Amended Claim 1 and on the above remarks.

Reconsideration of Claims 6 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on Amended Claim 1, Canceled Claim 7, and on the following remarks.

Applicant respectfully submits that it would have not been obvious to one skilled in the art at the time of the invention to combine the scrambling and descrambling techniques taught by Anderson and by Oshawa with the teachings of Lu to produce the claimed invention as recited in Amended Claim 1. In particular, the cited art does not appear to teach or to suggest this key feature. Applicant teaches in the Specification, pages 13 and 14 the following:

"The BIST Controller 60 sends out the memory data, address, and commands in the data bus, BDIN 61. The BDIN bus 61 is processed through a Data/Address "Scramble" Block 64 before entering the Embedded Memory Behavioral Model 84. The

Data/Address "Scramble" Block 64 is a key feature of the present invention. The BIST Controller 60 may be a generic circuit. Therefore, the logical arrangement of the BDIN bus 61 information is fixed. The "Scramble" block maps the logical configurations of the BDIN bus 61 onto the physical architecture used in an embedded memory. The Data/Address "Scramble" Block outputs the data bus in correctly scrambled format as BDIN_S. The Data/Address "Scramble" block 64 increases the flexibility of the verification method and apparatus of the present invention.

The Embedded Memory Behavioral Model 84 will be described in detail below. The output of the Embedded Memory Behavioral Model 84 is the bus BDOUT_S 66. Once again, this bus is "scrambled" with respect to the logical arrangement expected by the generic BIST design. Therefore, a Data/Address "Descramble" Block 68 is used to rearrange the BDOUT_S bus 66 to the appropriately "descrambled" BDOUT 69. This is another important feature of the preferred embodiment."

The need to descramble or rearrange the output BDOUT_S 66 of the behavioral model 84 to thereby generate BDOUT 69 prior to comparing data in the BIST comparitor 72 is taught only by the Applicant. Lu, Anderson, and Ohsawa, either separately or in

combination, do not teach or suggest this key feature of Applicant's claimed invention as recited in Amended Claim 1. Further, the cited art does not appear to provide a motivation to combine the teachings regarding digital logic circuits in Anderson or Ohsawa with the teachings regarding a behavioral model in Lu.

Applicant believes that Amended Claim 1 is not unpatentable over Lu in view of and further in view of Anderson for the above reasons. Claim 7 has been canceled. Finally, Claim 6 represents a patentably distinct, further limitation on Amended Claim 1 and should be in condition for allowance if Amended Claim 1 is not rejected under 35 U.S.C. 103(a).

Reconsideration of Claims 6 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on Amended Claim 1, Canceled Claim 7, and on the above remarks.

Reconsideration of Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on the following remarks.

As discussed above, Applicant believes that Amended Claim 1 is not unpatentable over Lu in view of and further in view of Anderson for the above reasons. Similarly, Claim 8 should not be unpatentable over Lu in view of and further in view of Anderson because Claim 8 already contains the limitation regarding the use of descrambling contained in Amended Claim 1.

Reconsideration of Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on the above remarks.

Reconsideration of Claims 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on the following remarks.

As stated above, Applicant believes that Claim 8 should not be unpatentable over Lu in view of and further in view of Anderson because Claim 8 already contains the limitation regarding the use of descrambling contained in Amended Claim 1. Further, Claims 9-12 represent patentably distinct, further

limitations on Claim 8 and should be in condition for allowance if Claim 8 is not rejected under 35 U.S.C. 103(a).

Reconsideration of Claims 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on the above remarks.

Reconsideration of Claims 18 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on Amended Claim 13 and on the following remarks.

The discussion above in regards to Amended Claim 1 applies also to Amended Claim 13. Claim 13 has been amended to read as follows:

13. (Currently Amended) An apparatus to verify the performance of a built-in self test circuit for testing embedded memory in an integrated circuit device comprising:

an embedded memory behavior model wherein said embedded memory behavior model comprises a high-level language model;

a built-in self-test circuit model connected to said embedded memory behavior model wherein said built-in self-test circuit model generates input data and address patterns for said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are compared to said input address and data in said built-in self-test circuit and a fault output is generated if not matching;

a means of introducing a set of faults into said embedded memory behavior model wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;

a means of simulating said embedded memory behavior model and said built-in self-test circuit model;

a means of de-scrambling said set of faults; and

a means of comparing the fault diagnosis output of said built-in self-test circuit model and said set of faults to verify the performance of said built-in self-test circuit.

As discussed in regards to Amended Claim 1, the need to descramble or rearrange the output BDOUT_S 66 of the behavioral

model 84 to thereby generate BDOUT 69 prior to comparing data in the BIST comparitor 72 is taught only by the Applicant. Lu, Anderson, and Ohsawa, either separately or in combination, do not teach or suggest this key feature of Applicant's claimed invention as recited in Amended Claim 13. Further, the cited art does not appear to provide a motivation to combine the teachings regarding digital logic circuits in Anderson or Ohsawa with the teachings regarding a behavioral model in Lu.

Applicant believes that Amended Claim 13 is not unpatentable over Lu in view of and further in view of Anderson for the above reasons. Claim 19 has been canceled. Finally, Claim 18 represents a patentably distinct, further limitation on Amended Claim 13 and should be in condition for allowance if Amended Claim 13 is not rejected under 35 U.S.C. 103(a).

Reconsideration of Claims 18 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of Ohsawa (U.S. Patent 5,742488) and further in view of Anderson (U.S. Patent 4,782,488) is requested based on Amended Claim 13 and on the above remarks.

Reconsideration of Claim 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of SyTest

Technologies, Inc., March 1999, is requested based on Amended Claim 13 and on the following remarks.

Applicant believes that neither Lu nor SyTest teach or suggest, separately or in combination, the key element of de-scrambling the set of faults as is taught in Applicant's claimed invention per Amended Claim 13. Therefore, Applicant does not believe that it would have been obvious to one skilled in the art at the time of the invention to have used the teachings of Lu and/or SyTest to practice the claimed invention.

Reconsideration of Claim 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (U.S. 6,012,157) in view of SyTest Technologies, Inc., March 1999, is requested based on Amended Claim 13 and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

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